AUSTRIAN INSTITUTE OF TECHNOLOGY
TOMORROW TODAY

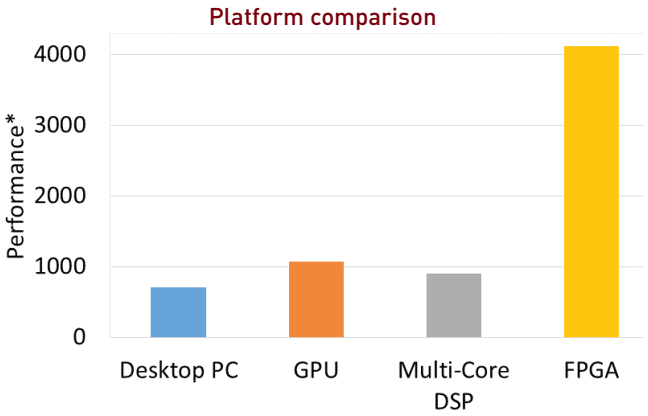
S³E FPGA

HIGH SPEED STEREO ENGINE

TECHNOLOGY

The FPGA Stereo Engine (S³E) is a highly scalable real-time stereo matching system for high quality depth image generation.

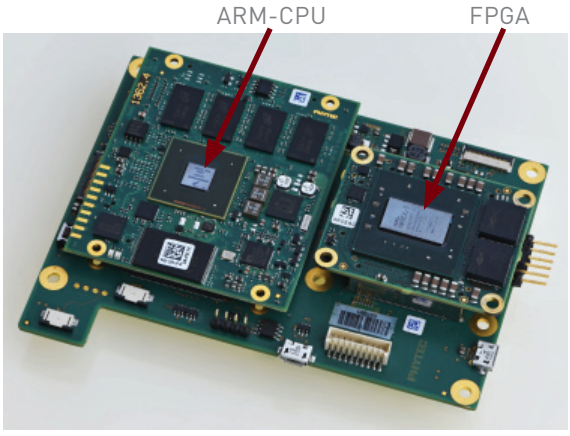
S³E FPGA addresses developers of (embedded) computer vision systems for real-time 3D applications. The stereo vision core performs stereo matching on two grayscale input images. First, the images are rectified to compensate for lens distortions and camera alignment errors. Stereo matching is then performed by applying a special variation of the census transform, which delivers enhanced result quality. The output of the stereo vision core is a subpixel accurate and dense disparity map (an inverse depth map).



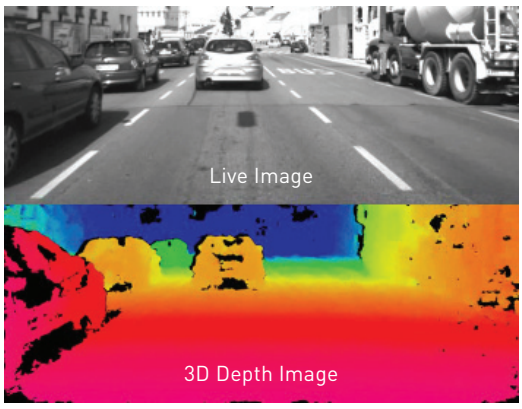
*) Million disparity evaluations per second. Test - image size 450x375 pixels, 60 disparities. Desktop PC: Intel i7 with 4x2 Cores and 3GHz; GPU: GTX280 with 240 Cores and 1.3GHz; Multi-Core DSP: TMS320C6678 with 8 Cores and 1GHz; FPGA: XC7Z020 with 150MHz.

HIGHLIGHTS

- Licensable IP core
- Development of prototypes for integrated custom solutions:
  - Embedded system design including FPGA and ARMs/ x86
  - Embedded real-time video processing
- High performance and low-power
- Sophisticated stereo engine outperforms conventional stereo algorithms
- Algorithm is highly configurable for easy adoption
- Flexible disparity range
- Image resolution can be dynamically set
- Various fields of applications



FPGA calculates high quality depth images in real-time



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PORTFOLIO

PCIe-based Solution

- Reference implementations for standard x86 based desktops and ARM-based industrial PCs
- Software module: Executable with demo framework or static libraries with C/C++-API
- Arbitrary platforms providing PCIe are supported

Embedded Solution

- Highly integrated and small form factor for embedded vision processing and smart camera platforms
- Reference implementations for Zynq FPGAs

APPLICATIONS

Stereo vision technology is used in a variety of applications, including people and object tracking, robotics, as well as autonomous vehicles. It is also used in industrial production and inspection applications to perform tasks such as bin picking, volume measurement, automotive part measurement and 3D object localization and identification.

TECHNICAL SPECIFICATION

Input	Stereo image pairs of arbitrary resolution (up to 1920x1080), grayscale (up to 16bpp)
Output	Disparity (subpixel accurate), 16bpp, fixed-point format
S³E	Rectification and stereo processing completely on FPGA
Census Mask	Various types with correlation mask size up to 16x16
Versatility Features	▶ Asymmetric 3-camera configurations for optimized depth range and accuracy ▶ Hierarchical stereo matching mode boosts performance and accuracy ▶ Support for tilted camera pairs enables wide and accurate stereo baselines ▶ Image resolution can be dynamically set ▶ Flexible disparity configuration (depending on available FPGA resources)
Scalability	FPGA selection depending on specific requirements
Platforms	▶ PCIe PC (Intel x86, Windows & Linux) ▶ PCIe industrial PC (ARM, Linux) ▶ Zynq (ARM, Linux)

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